REMARKS

The Office Action mailed April 9, 2003 has been carefully reviewed and the foregoing amendment has been made in consequence thereof. Submitted herewith is a Submission of Marked Up Claims.

Claims 1-24 are now pending in this application. Claims 6-9 are withdrawn from consideration. Claims 10-21 are allowed. Claims 1-4, 22, and 23 stand rejected. Claims 5 and 24 are objected to.

The rejection of Claims 1-4, 22, and 23 under 35 U.S.C. § 103 as being unpatentable over Applicants Specification in view of Palmour et al. (High-temperature Depletion-mode Metal-oxide-semiconductor Field-effect Transistors in beta-SiC Thin Films, Dec. 1987) and Slater, Jr. et al. (6,344,663) is respectfully traversed.

Claim 5 was indicated in the Office Action as being allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claim 5 depends indirectly from Claim 1. Claims 2 and 5 have been cancelled and independent Claim 1 has been rewritten to include all of the recitations from Claims 2 and 5. Accordingly, Claim 1 is submitted to be in condition for allowance, and as such, is submitted as patentable over Applicants Specification in view of Palmour et al. and Slater, Jr. et al.

Claim 24 was indicated in the Office Action as being allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claim 24 depends indirectly from Claim 22. Claims 23 and 24 have been cancelled and independent Claim 22 has been rewritten to include all of the recitations from Claims 23 and 24. Accordingly, Claim 22 is submitted to be in condition for allowance, and as such, is submitted as patentable over Applicants Specification in view of Palmour et al. and Slater, Jr. et al.

For the reasons set forth above, Applicant respectfully requests that the rejection of Claims 1-4, 22, and 23 under 35 U.S.C. § 103 be withdrawn.

In view of the foregoing amendments and remarks, all the claims now active in this application are believed to be in condition for allowance. Reconsideration and favorable action is respectfully solicited.

Respectfully Submitted,

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Express Mail No. EV 339985882 US

RD-27645
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Donald Thomas McGrath

Serial No.: 09/682,863

Filed: October 25, 2001

For: METHODS AND APPARATUS FOR AMPLIFICATION IN HIGH TEMPERATURE ENVIRONMENTS

Art Unit: 2817

Examiner: Shingleton, Michael B.

SUBMISSION OF MARKED UP CLAIMS

Hon. Commissioner for Patents
Mail Stop: NON-FEE AMENDMENT
P.O. Box 1450
Alexandria, VA 22313-1450

Submitted herewith are marked up Claims in accordance with 37 C.F.R. 1.121(c)(1)(ii), wherein additions are underlined and deletions are [bracketed].

IN THE CLAIMS

Please cancel Claims 2, 5, 23, and 24

1. (twice amended) A method for amplifying a signal comprising:

generating an input signal; [and]

amplifying the input signal utilizing a chopper-stabilized, silicon carbide NMOS depletion mode operational amplifier to produce an amplified output signal, the operational amplifier including a first NMOS depletion mode amplification stage and a second NMOS

depletion mode amplification stage, the first stage and the second stage fabricated on the same silicon carbide substrate, wherein amplifying the input signal comprises chopping the input signal utilizing a first NMOS depletion mode chopping switch responsive to a first chopping signal to produce a first chopped input signal; and

generating at least one opposite node of a resistor of an NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit, the first chopping signal, and the level shifted first chopping signal in response to a clock signal.

22. (once amended) A method for amplifying a signal comprising:

generating an input signal;

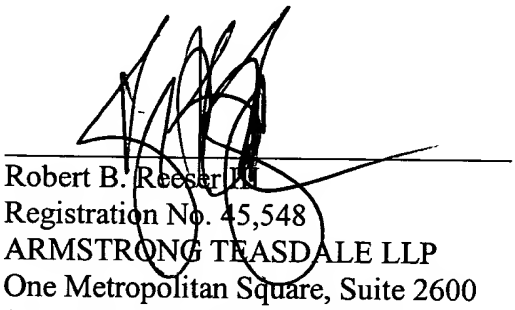
amplifying the input signal utilizing a chopper-stabilized, silicon carbide NMOS depletion mode operational amplifier responsive to a level shifted first chopping signal to produce [an amplified] a chopper-stabilized output signal output signal;

amplifying the input signal by chopping the input signal utilizing a first NMOS depletion mode chopping switch that is responsive to a first chopping signal to produce a first chopped input signal; [and]

amplifying the first chopped input signal utilizing an NMOS depletion mode amplifier stage to produce an amplified chopped output signal; and

generating, at opposite nodes of a resistor of an NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit, the first chopping signal and the level shifted first chopping signal in response to a clock signal.

Respectfully Submitted,



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